UTTARAKHAND OPEN UNIVERSITY, HALDWANI (NAINITAL)
उत्तराखंड मुक्त विश्वविद्यालय, हल्द्वानी (नैनीताल)

PGDCA-11 1ST YEAR 1ST SEMESTER ASSIGNMENT

Last Date of Submission: 15 Jan. 2013

Course Title: Digital Logic **Course Code: PGDCA-02**
Year: 2012-13 **Maximum Marks: 40 Marks**

Section 'A'

Section 'A' contains 08 short answer type questions of 5 marks each. Learners are required to answers 4 questions only. Answers of short answer-type questions must be restricted to 250 words approximately.

1. Convert JK flip-flop to T-flip-flop.
2. Draw the state diagram of SR Flip Flop.
3. Mention the major application of Master Slave FF.
4. Describe the working of EPROM. List the applications of EPROM.
5. Discuss on the concept, operation and characteristics of CMOS technology.
6. Describe procedure to get state table from excitation table in an asynchronous sequential circuit. How does it differ from synchronous sequential circuit?
7. Draw and explain the working of 4 bit adder – subtractor circuit.
8. Explain with truth table and gate level circuits diagram for a full adder.

Section 'B'

Section 'B' contains 04 long answer-type questions of 10 marks each. Learners are required to answers 02 questions only.

1. Using SR flip-flops, design a synchronous counter which counts in the sequence 000, 111, 101, 110, 001, 010, 000
2. Discuss the working of the following programmable logic devices:
   i. PROM ii. FPGA iii. PLD
3. For the given function write the Boolean expression in product of maxterms form

f(a,b,c) = Σm (2,3,5,6,7)

4. Determine the prime implicants of the following function and verify using K-map
F(A,B,C,D) = Σ(3,4,5,7,9,13,14,15)